Amendments to the Specification:

Please replace the paragraph **[0017]** with the following rewritten paragraph **[0017]**:

[0017] Fig. 2 illustrates an exemplary embodiment of the present invention comprising the two format converters 234 and 244 each processing one-half of the active video field 122. The exemplary converters 234 and 244 are coupled to a controller 235 that synchronizes the two controllers but otherwise allows each controller to process its respective half video field independently of the processing of the other converter. The embodiment shown in Figure 2 reduces the delay time expended converting from the input video signal 120 into the output video signal 160. The system operates by applying the input video signal 120 to an input formatter 121 that splits each field of the input video signal into two overlapping half-fields 212 and 222. The two fields are processed by the respective format converters 234 and 244 to produce respective output signals 250 and 260. These signals are combined in an output ~~demultiplexer~~ multiplexer 251 to generate the output signal 160.. In the exemplary embodiment of the invention shown in Figure 2, the first video signal 210 includes the top half 212 of field 122 while the second video signal 220 includes the bottom half 222 of field 122.

B1 cont.

Please replace the paragraph **[0027]** with the following rewritten paragraph **[0027]**:

[0027] As shown in the timing diagrams 234T and 244T, the format converter 234 processes the top half interval 212 between times T4 and T6 while the format converter 244 processes the bottom half interval 222 between times T5 and T7. Between times T6 and T8, the format converter 234 provides the converted top half interval 252 of field N in its output signal 250. Between times T7 and T9, the format converter 244 provides the converted bottom half interval 262 of field N in its output signal 260. The signal provided by both converters 234 and 244 between the intervals T7 and T8 is the overlap region, described below with reference to Figs. 3 and 3A. The output signals 250 and 260 are combined by the ~~demultiplexer~~ multiplexer 251 to produce the converted field N between times T6 and T9.

B2 cont.